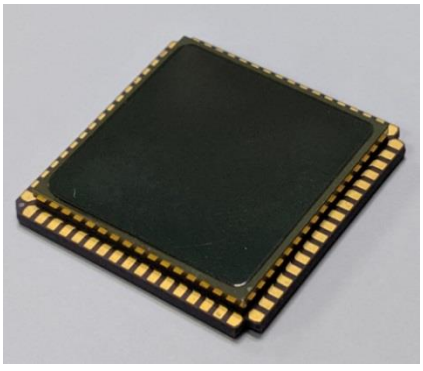
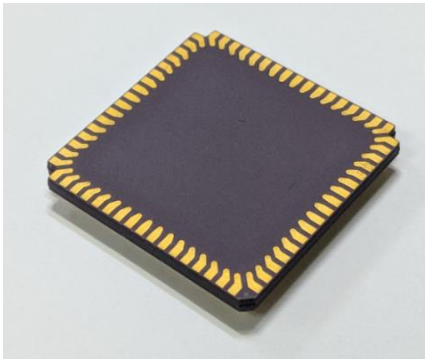
160×120 Uncooled Bolometer FPA

FEATURES

- 160×120 pixels, 52 micron pitch
- Low noise VOx technology
- Optimized for the 8-14 micron spectral region (other regions are also possible)
- Fully integrated, low noise on-chip CMOS readout electronics
- Pulsed current bias, single analog output
- Random and self-scanning pixel addressing modes
- On-chip temperature drift and offset compensation
- On-chip noise filtering
- Mounted in an evacuated package, complete with 8-14 micron AR-coated germanium window
- 68LCC Ceramic Substrate Package size: 24.13mm x 24.13mm x 3.16mm (with 1mm window)



Top Side View



Back Side View

DESCRIPTION

The GTM160 is a robust and adaptable uncooled bolometer array composed of 19,200 independent pixels, arranged in a square matrix of 160 x 120 pixels. The dimension of each pixel is 50 x 50 microns, with a pitch of 52 microns. Each bolometer resistance is made from VOx thermistor. A set of 4 reference pixels is provided to perform optional coarse offset and temperature drift compensation. The packaged arrays are optimized for operation in the 8 to 14 micron infrared optical region, making them ideal for passive detection of radiation emitted by targets. By using different window materials, the arrays can be optimized for operation at other wavelengths.

The GTM160 integrated readout electronics provides a simple clocking and readout arrangement.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating			Unit
		Min.	Typ.	Max	
Supply voltage[1]	VDD	4.5	5	5.5	V
Supply current	IDD		75	90	mA
Data frequency	FVOUT	DC	576	2000	kHz
Frame rate	fframe		27.9		Hz
Operating ambient temperature[2]	TOP	-35	+25	+65	℃
Maximum case temperature	TCASE			+45	℃
Storage temperature	TSTG	-55		+80	℃

Table 1: Absolute Maximum Ratings

[1] VDD lines (VDD, VDD_PIXEL and VDD_ANA) must all be at the same voltage level.
[2] The ultimate ambient temperature that is possible is a function of specific thermal design.

LOGIC BLOCK DIAGRAM

Figure 1. shows the logic block diagram of the GTM160. Only the major signals are illustrated. Power and temperature sensors have been omitted for simplification.

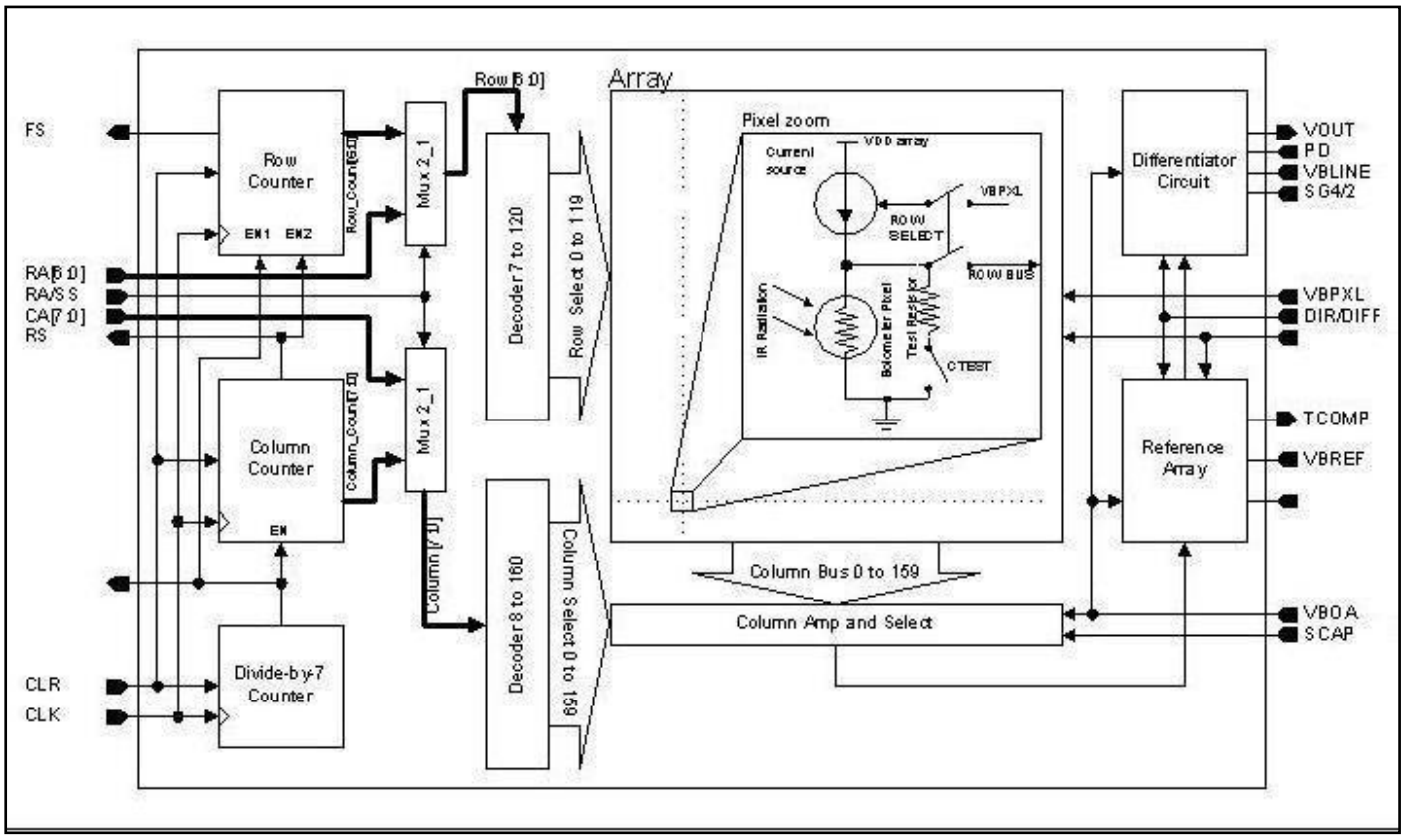


Figure 1: GTM160 Logic Block Diagram

PIN CONFIGURATION (PIN NO.1 in the upper left corner)

Top view

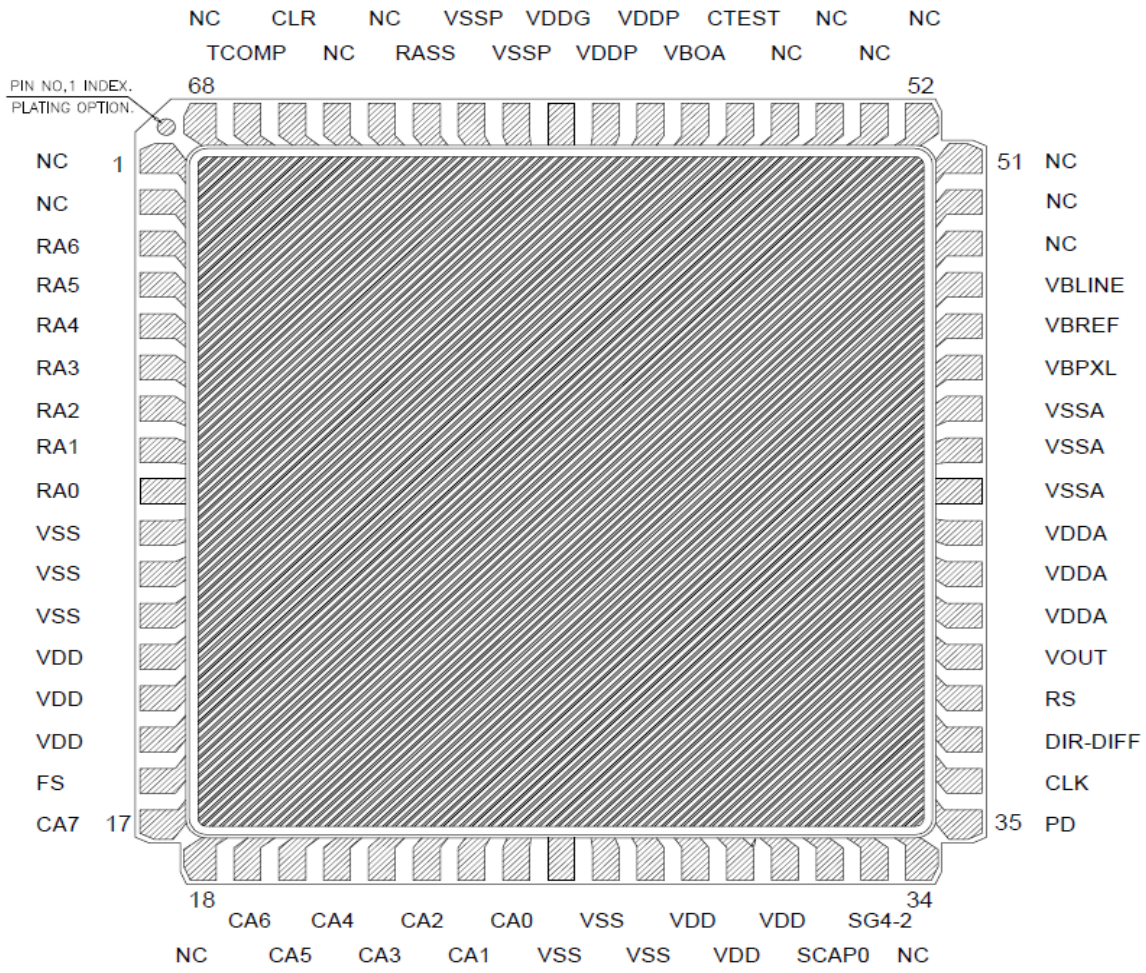
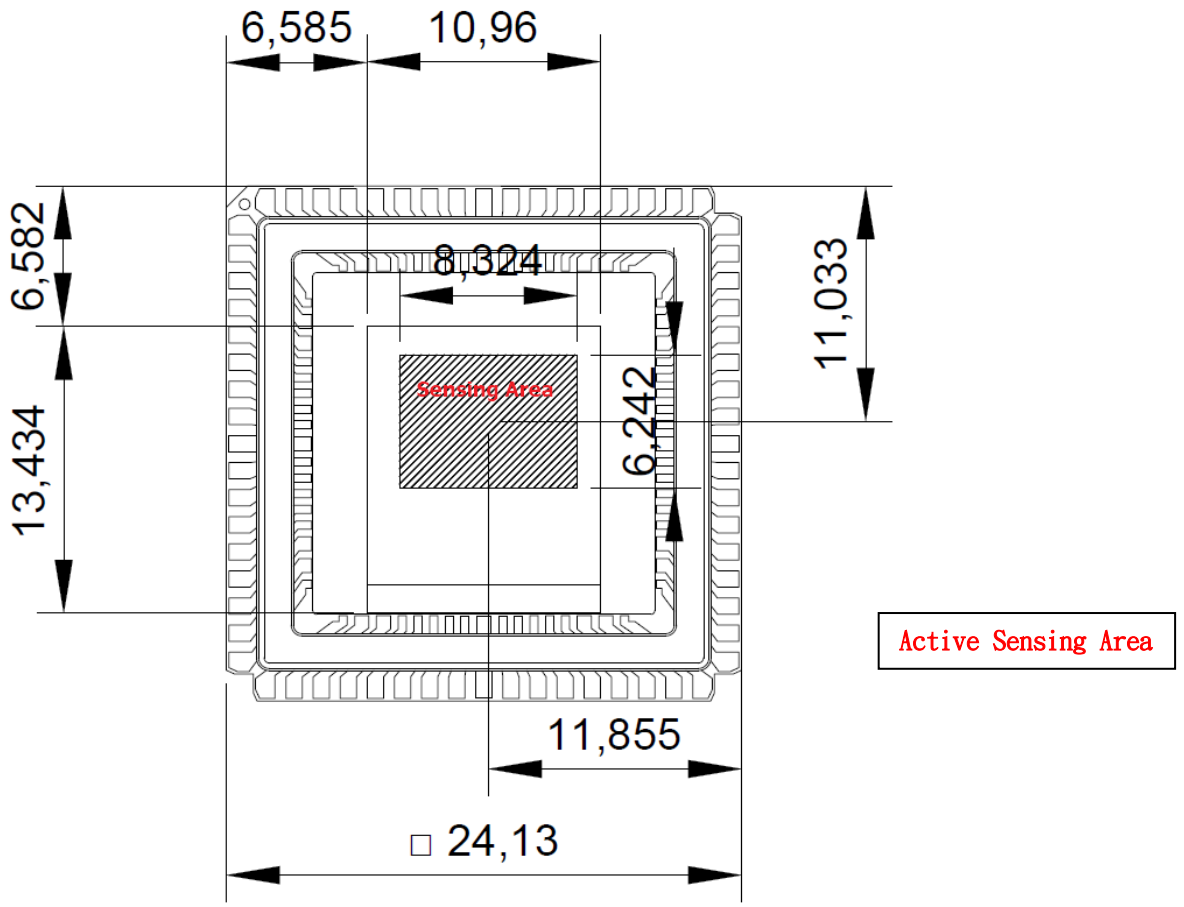


Figure 2: Pin Configuration of the GTM160 Package

Defined Active Sensing Area in 68LCC Package



Unit: mm

PIN DESCRIPTION

Pin NO.	Pin Name	Type	Description
3	RA6	Input	Row Address Input bit 6 (MSB) for addressing the rows of the array in Random Access mode.
4	RA5	Input	Row Address Input bit 5 for addressing the rows of the array in Random Access mode.
5	RA4	Input	Row Address Input bit 4 for addressing the rows of the array in Random Access mode.
6	RA3	Input	Row Address Input bit 3 for addressing the rows of the array in Random Access mode.
7	RA2	Input	Row Address Input bit 2 for addressing the rows of the array in Random Access mode.
8	RA1	Input	Row Address Input bit 1 for addressing the rows of the array in Random Access mode.
9	RA0	Input	Row Address Input bit 0 (LSB) for addressing the rows of the array in Random Access mode.
16	FS	Output	Frame Sync. High during the last row. The falling edge of indicates the beginning of anew frame.
17	CA7	Input	Column Address input bit 7 (MSB) for addressing the columns of the array in Random Access mode.
19	CA6	Input	Column Address input bit 6 for addressing the columns of the array in Random Access mode.
20	CA5	Input	Column Address input bit 5 for addressing the columns of the array in Random Access mode.
21	CA4	Input	Column Address input bit 4 for addressing the columns of the array in Random Access mode.
22	CA3	Input	Column Address input bit 3 for addressing the columns of the array in Random Access mode.
23	CA2	Input	Column Address input bit 2 for addressing the columns of the array in Random Access mode.
24	CA1	Input	Column Address input bit 1 for addressing the columns of the array in Random Access mode.
25	CA0	Input	Column Address input bit 0 (LSB) for addressing the columns of the array in Random Access mode.
26,27,28	VSS	Power	Digital ground.
29,30,31	VDD	Power	Digital supply voltage.
32	SCAP	Input	On-chip filtering switch control. Set high to enable internal filtering capacitor.
33	SG4/2	Input	Output gain in Differential Output mode. Gain is 4 when set high, and 2 when set low. Set low in Direct Output Mode.
35	PD	Input	Power-down control of the output amplifier.
36	CLK	Input	Crystal controlled Clock input.
37	DIR/DIFF	Input	Output mode select. Set high for Direct output mode, and low for Differential Output mode.
38	RS	Output	Row Sync output. High on last pixel of the current row.
39	VOUT	Analog Out	Select pixel output of the active array (1V~3V) **Warning**: Shorting the video output to VSS or VDD can permanently damage the output amplifier.
40,41,42	VDDANA	Power	Analog supply voltage (5V)
43,44,45	VSSANA	Power	Analog ground.
46	VBPXL	Analog In	Active pixel input bias voltage (2V~5V)
47	VBREF	Analog In	Reference pixel input bias voltage (2V)
48	VBLINE	Analog In	Output baseline voltage input (2.5V)

57	VBOA	Analog In	Operational amplifier bias input (3.9V)
60,59,58	VDDP	Power	Pixel supply voltage (5V)
61,62	VSSP	Power	Pixel ground.
63	RA/SS	Input	Random Access/Self Scanning mode. Set to select Random Access.
64	NC	NC	NC
65	NC	NC	NC
66	CLR	Input	Counters asynchronous clear.
67	TCOMP	Analog Out	Temperature compensation signal.

Table 2: GTM160 Pin Description

ADDRESSING MODES

The GTM160 Readout offers two modes for accessing the pixels of the detector.

The pixels can be addressed in a Random Access Mode where the signal corresponding to a particular micro-bolometer is directed to the output only when its address is received by the detector. This mode offers considerable readout flexibility and allows arbitrary subsections of an array to be addressed. All pixels can be addressed individually using the address pins CA[7:0] and RA[6:0]. Address pins CA[7:0] and RA[6:0] are internally pulled down.

Alternatively, the rows and columns of the array can be scanned sequentially at rates determined by the applied clock frequency. This mode is called Self Scanning Clocking. In this mode, the Column Counter and the Row Counter are clocked by the signal on the CLK pin. This can be accomplished by feeding the CLK input with a clock frequency 7 times the desired column scan rate. This way, a complete self-scanning with a single clock input applied to CLK can be accomplished.

Selection of the Random Access and Self Scanning modes depend on the states of the RA/SS (Random Access /Self Scanning) pin as shown in table 4.

Clocking Mode	RA/SS	Remark
Self Scanning	Low	Pixels are sequentially scanned. Uses the CLK input.
Randm Access	High	Row and Column address of the pixel selected by RA[6:0] and CA[7:0].

Table 3: Clocking Mode Truth Table

CLOCK GENERATION AND READOUT

The internal counters of the GTM160 provide pixel address generation (Row Counter and Column Counter) and clock dividing (Divide-by-7 Counter) for the Self Scanning Clocking mode. All counters respond to the rising edge of their respective clock input. The counters will not start to count until a clear pulse is applied to them. Clear pulse is applied through the CLR pin. The relation between the framerate and the master clock frequency is given by:

$$f_{FrameRate} = \frac{f_{CLK}}{7*19,200};$$

For example, a CLK frequency of 4 MHz would generate 29.76 frames per second. Refer to the TIMING section for more details on clock generation timings.

BIAS VOLTAGE AND BIAS CURRENT

The voltage applied to pin 35 VBPXL is the voltage applied to the gate of the current source transistor of each pixel (VBREF for the reference pixel). VBPXL and VBREF should be a low noise input with respect to VDD. Maximum recommended noise levels are 0.1mV RMS for low frequency, or 1µV RMS for high frequency noise above 3KHz. high frequency noise above 3 KHz.

Nominal value of bias voltage on pin VBPXL and VBREF is VDD_PIXEL 3.5Volts. The design nominal values are 50kΩ pixel resistance with a 40µA bias current.

The relation between the bias voltage and the continuous bias current is given by:

$$I_{bias}(\mu A) = \frac{\beta_p}{2}\left(V_{DD} - V_{BPXL} - |V_{THp}|\right)^2;$$

Where V_{DD} is VDD_PIXEL, β_p is the transconductance and VTHp is the threshold voltage of the P-channel transistor of the current source.

Approximate values for ßp and VTHp are 11.17 mA/V2 and –0.834 V respectively.

The voltage applied to pin 57 VBOA is the Operational amplifier bias voltage input. Nominal value of bias voltage on pin VBOA is VDD_ANA-1.1 Volts. Noise level on VBOA has the same restrictions than on VBPXL and VBREF, which are less than 0.1mV RMS for low frequency noise and less then 1µV RMS for high frequency noise above 3kHz.

TEMPERATURE COMPENSATION

The GTM160 has a temperature compensation feature which can be used to compensate for the die temperature drift. A small reference pixel set composed of surface-mounted temperature-sensing bolometer, represents the average die temperature. The signal from the surface bolometers, corresponding to the average die temperature, is subtracted from the value read from a selected active pixel. This removes the effect of background temperature variations from the output signal of the array to a first order.

The reference pixel set is composed of 4 pixels. There is one pixel on each side of the array. Each temperature-sensing pixel is supplied by its own current source. Current sources are not pulsed but continuously biased, because the reference pixels are always selected when operating in Differential mode. Bias voltage at the gate of the current source transistor is applied at pin VBREF. Reference pixels are activated four at a time, one on each side. The four temperature reference signals are averaged before subtraction.

The subtraction of the temperature signal from the reference pixel array takes place in an internal differentiator circuit. One input is connected at the output of every column amplifier, and the other at

averaged before subtraction.

The subtraction of the temperature signal from the reference pixel array takes place in an internal differentiator circuit. One input is connected at the output of every column amplifier, and the other at the averaged temperature reference signal. Only the output of the selected column amplifier is present at the differentiator circuit. The differentiator circuit also allows to add an offset voltage (applied at pin VBLINE) and an output gain (selected at pin SG4/2). The temperature-compensated output is available at pin VOUT. To allow an external compensation circuit, the output of one reference pixel is available at pin TCOMP.

The temperature compensation feature is enabled via pin DIR/DIFF. When set low, the output signal pin VOUT is temperature compensated with the previously described differentiator circuit. When high, the temperature-sensor array is not activated, and the active pixel signals that outputs the selected column amplifier bypasses the differentiator circuit, so the output VOUT is not temperature compensated.

The output relations are given in table 5:

Mode	Gain	DIR/ DIFF	SG4/ 2	VOUT
Differential	2	0	0	2 × (BUSPLX-BUSREF) + VBLINE
	4	0	1	4 × (BUSPLX-BUSREF) + VBLINE
Direct	1	1	0	BUSPLX + VSS_ANA
	1	1	1	Not used

Table 4: Operation Modes and Corresponding Output

Where BUSPLX is the output voltage signal of the selected pixel, and BUSREF is the averaged temperature reference signal.

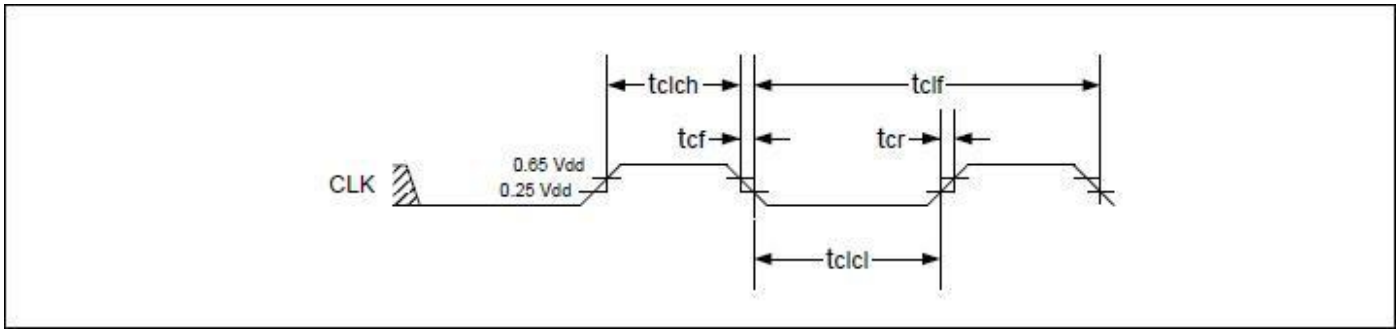
ON-CHIP NOISE FILTERING

An internal filter may be enabled to reduce the bandwidth when the GTM160 is operated at 30Hz or less. External filtering may be added, if carefully designed for the best trade off between NETD and MRTD.

TIMING

SYSTEM CLOCK

Parameter	Symbol	Rating			Unit	Notes
		Min.	Typ.	Max.		
Clock Frequency	f_C	1.3	4	13.4	MHz	
Clock Rising Time	t_{CR}		1.2		ns	
Clock Falling Time	t_{CF}		1.4		ns	



COUNTER'S RESET

Parameter	Symbol	Rating			Unit	Notes
		Min.	Typ.	Max.		
Reset signal (set or preset) pulse width	t_{WRST}		2		μs	
End of reset before clock pulse	t_{EBC}		178		ns	

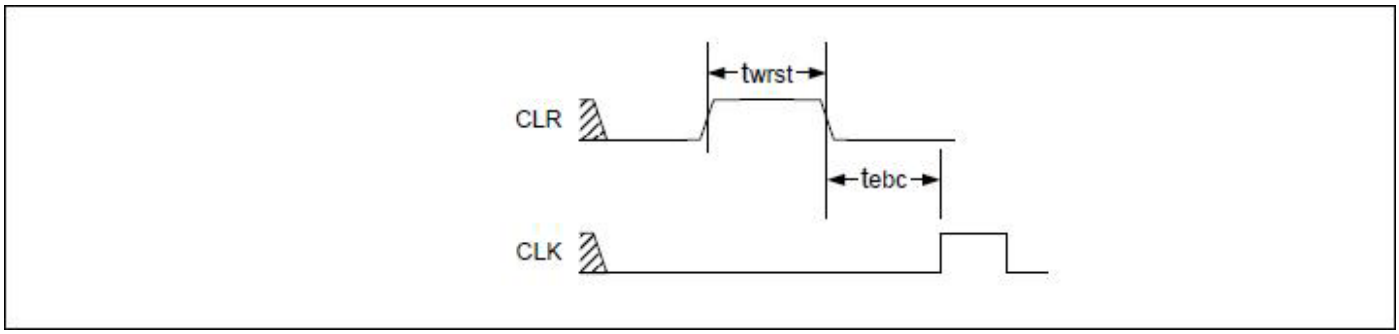
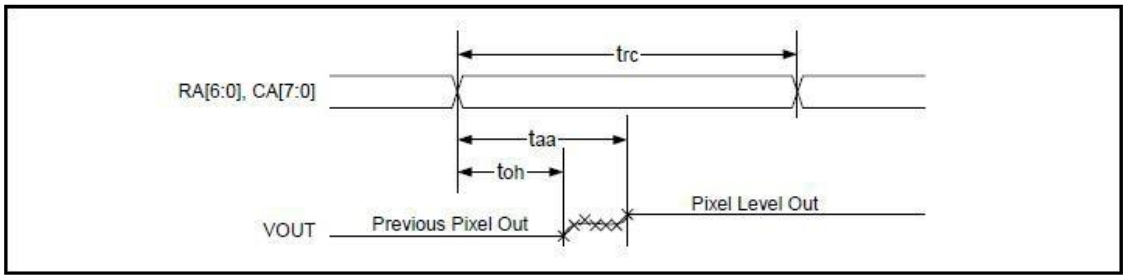


Figure 3: System Clock Timing

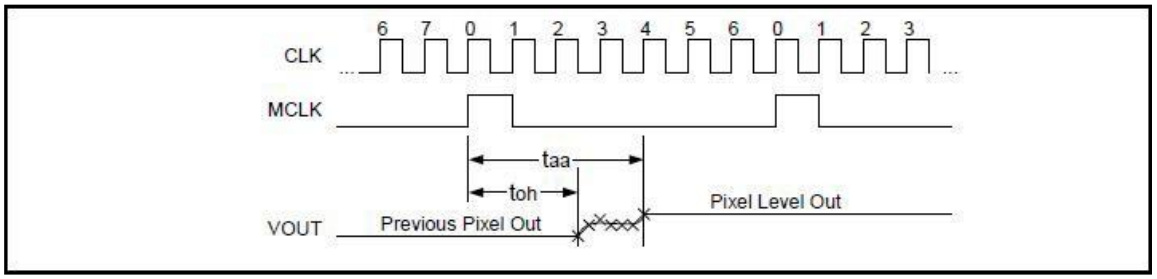
RANDOM ACCESS READ

Parameter	Symbol	Rating			Unit	Notes
		Min.	Typ.	Max		
Read cycle time	t_{RC}		1.7		μs	
Address access time	t_{AA}	330	470	560	ns	
Output hold from address change	t_{OH}	60	70	85	ns	



SELF CLOCKING MODE READ ACCESS

Parameter	Symbol	Rating			Unit	Notes
		Min.	Typ.	Max		
Read cycle time	t_{RC}		1.7		μs	
Address access time	t_{AA}	560	640	690	ns	
Output hold from address change	t_{OH}	200	230	250	ns	



SIGNAL BEHAVIOR, PIXEL AND ROW CLOCKING NODE

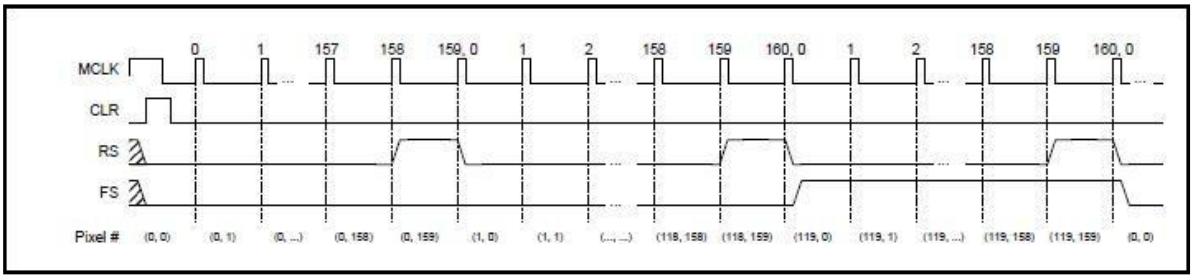


Figure 4: Readout Timing

Package Information